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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,034	12/27/2001	Kenneth C. Creta	10559-639001 / P12351	9181

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	9

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/035,034	Applicant(s) CRETA ET AL.	
	Examiner Midys Inoa	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on August 11th, 2003 has been considered by the examiner.

Drawings

2. The replacement drawing was received on November 12, 2003. The replacement drawing has been accepted by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 and 8-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780) in view of "The Cache Memory Book" by Jim Handy.

Regarding Claims 1-6 and 10, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity filed 144 ("validity bit storage") keeps track of which of the thirty-two portions of each storage location has been written to and when all are full, the storage location ("cache line") is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines 1-30). Glew et al. also discloses that storage in the buffer 132 is very much like storage on an on-chip cache unit (DCU), therefore, as

DCU's, buffer 132 may store data corresponding to locations in main memory (See Column 1, lines 25-38 and Column 7, lines 30-32). Glew et al. does not teach buffer 132 being part of a coherency protocol. Handy teaches cache coherency which prevents stale data from being confused with current data (page 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the cache coherency of Handy to the buffer of Glew et al. since this buffer behaves much like a cache and adding such protocol would prevent the confusion between good and useless data. **It is understood that in integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; adding such delays would be a tradeoff to be paid for the ability to differentiate between stale and current data.**

Regarding Claim 11, Glew et al. also discloses an eviction mechanism for an on-chip data cache unit in which a cache line is evicted when it is determined that the cache line is full. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the details of the buffer eviction policy disclosed by Glew et al. to accomplish the cache eviction policy since the buffer of Glew et al. behaves much like a usual cache and employing such eviction policy would be very efficient and easy to implement.

Regarding Claims 8, 14, Glew et al. teaches transmitting evicted data through bus unit 130 to an external destination device, which could be a frame buffer or a separate memory (See Column 7, lines 47-52).

Regarding Claims 9, 16, Glew et al. teaches a Write Combining Unit 138 ("input/output device") which provides the data written into the storage locations of buffer 132 (See Figure 4 and Column 7, lines 15-30).

Regarding Claims 13, 15, 18 22-26 and 28, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") being written to through the use of a write combining unit 138, and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity filed 144 ("validity bit storage") keeps track of which of the thirty-two portions of each storage location has been written to and when all are full, the storage location ("cache line") is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines 1-30). Glew et al. also discloses that storage in the buffer 132 is very much like storage on an on-chip cache unit (DCU), therefore, as DCU's, buffer 132 may store data corresponding to locations in main memory (See Column 1, lines 25-38 and Column 7, lines 30-32). Glew et al. does not teach buffer 132 being part of a coherency protocol. Handy teaches cache coherency which prevents stale data from being confused with current data (page 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the cache coherency of Handy to the buffer of Glew et al. since this buffer behaves much like a cache and adding such protocol would prevent the confusion between good and useless data. **It is understood that in integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; adding such delays would be a tradeoff to be paid for the ability to differentiate between stale and current data. Additionally, although the write transaction of Glew et al. are not initiated directly by a input/output device, these transactions, which are initiated by a microprocessor, could be initiated indirectly, through the microprocessor, by the input/output device 125 (Figure 3).**

Regarding Claims 17 and 21, Glew et al. teaches filling cache-line size storage location with a number of combining partial writes and evicting one full storage location using a burst eviction. Therefore, is understood that if more than one write fills a storage location and only one eviction procedure evicts the same storage location, more writes must be executed for each eviction (Column 5, lines 20-33 and Column 7, lines 1-14).

Regarding Claim 19, Glew et al. does not teach using an additional write combining unit or I/O device to store additional data onto the buffer 132. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add another inputting unit to the write combining buffer of Glew et al. since such additional inputs would be integrated into the existing eviction system with ease and adding such additional inputs would give the system the ability to process more data.

Regarding Claims 12, 20 and 27, Handy discloses the workings of a MESI cache coherency protocol (pages 156-158).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780) in view of "The Cache Memory Book" by Jim Handy further in view of Van Huben et al. (2002/0083243 A1). Glew et al. in view of "The Cache Memory Book" teaches the invention as set forth by claim 1 above. Glew et al. in view of "The Cache Memory Book" does not teach evicting even if the storage location is not full, as long as there are no other evictions taking place at the same time. Van Huben et al. teaches allowing an initial LRU cast-out operation ("eviction") to complete while all other operations wait. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the wait policy employed in Van Huben et al. to the invention of Glew et al. in view of "The Cache Memory

Book" since such modification would prevent deadlocks or execution conflicts (pages 8-9, paragraph 112).

Response to Arguments

6. Applicant's arguments filed on November 12th, 2003 have been fully considered but they are not persuasive.

Regarding the arguments for Claims 1 and 10, **it is understood that in integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; adding such delays would be a tradeoff to be paid for the ability to differentiate between stale and current data.**

Regarding the arguments for Claim 22, **it is understood that in integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; adding such delays would be a tradeoff to be paid for the ability to differentiate between stale and current data. Additionally, although the write transaction of Glew et al. are not initiated directly by a input/output device, these transactions, which are initiated by a microprocessor, could be initiated indirectly, through the microprocessor, by the input/output device 125 (Figure 3).**

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa

Midys Inoa
Examiner
Art Unit 2188

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2/9/04

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TC 2100